NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

SEMESTER: I

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ETC	ET41111VL	Semiconductor Devices	3	1	-	20	15	15	100		150	4
2	ETC	ET41112VL	Advanced VLSI Design	3	1	-	20	15	15	100		150	4
3	ETC	ET41113VL	Introduction to CAD tools	2	0	3	20	15	15	100		150	4
4	ETC	ET41114VL	Digital IC Design	3	1	-	20	15	15	100		150	4
5	ETC	ET41121VL	Design Lab - 1	1	-	5	100	-	-	-	100	200	4
6	ETC	ET41122VL	Digital Design Lab	1	-	5	100	-	-	-	100	200	4
			Total	13	3	13	280	60	60	400	200	1000	24

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION

SEMESTER: II

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ETC	ET41211VL	Analog IC Design	3	1	-	20	15	15	100		150	4
2	ETC	ET41212VL	System on Programmable chip Design	3	1	-	20	15	15	100		150	4
3	ETC	ET41213VL	VLSI System Design	3	1	-	20	15	15	100		150	4
4	ETC	ET4123XVL	Elective 1	3	1	-	20	15	15	100		150	4
5	ETC	ET4124XVL	Elective 2	3	1	-	20	15	15	100		150	4
6	ETC	ET41221VL	Analog IC Design Lab	-	-	4	75	-	-	-	50	125	2
7	ETC	ET41222VL	System on Programmable Chip Design Lab	-	-	4	75	-	-	-	50	125	2
			Total	15	5	8	250	75	75	500	100	1000	24

ELECTIVE 1			
S. No.	Board of Studies	Sub Code	Subject Name
1	ETC	ET41231VL	Embedded Systems & RTOS
2	ETC	ET41232VL	Signal Processing Algorithms of DSP Architecture
3	ETC	ET41233VL	Mixed Signal Circuit Design
4	ETC	ET41234VL	Image processing and computer vision
5	ETC	ET41235VL	VLSI Technology

ELECTIVE 2			
S. No.	Board of Studies	Sub Code	Subject Name
1	ETC	ET41241VL	Advance Techniques in DSP
2	ETC	ET41242VL	MOS Device Modeling and Characterization
3	ETC	ET41243VL	Security solutions in VLSI
4	ETC	ET41244VL	Low Power VLSI Design Techniques
5	ETC	ET41245VL	MEMS

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DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION

SEMESTER: III

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ETC	ET4133XVL	Elective – 3	3	-	0	20	15	15	100		150	3
2	ETC	ET41321VL	Preliminary work on Dissertation	-	-	20	50	-	-	-	100	150	10
3	ETC	ET41322VL	Comprehensive viva-voce and seminar	-	-	-	-	-	-	-	200	200	3
			Total	3	0	20	70	15	15	100	300	500	16

ELECTIVE 3			
S. No.	Board of Studies	Sub Code	Subject Name
1	ETC	ET41331VL	Power device Modelling and application
2	ETC	ET41332VL	RF IC Design
3	ETC	ET41333VL	Nanoelectronics
4	ETC	ET41334VL	Design for testability, yield and reliability

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION

SEMESTER: IV

S.No.	BoS	Sub. Code	Subject Name	Periods/week			Examination Scheme					Total Marks	Credits L+(T+P)/2
				L	T	P	TA	FE	SE	ESE	Pract. ESE		
1	ETC	ET41421VL	Dissertation	-	-	32	200	-	-	-	300	500	16
			Total	-	-	32	200	-	-	-	300	500	16

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NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492

Department of Electronics and Telecommunication

"Semiconductor Devices"

Theory Periods: 30 Tutorials: "10

Credits: 4 Code: ET4111

Objective: The students should able to understand the basics of semiconductor phys. They can mathematically analyze PN junctions and MOSFETs. This course will also provi description of various semiconductor device models and parameters.

Course Content

UNIT I

Basic Semiconductor Physics: Crystal lattice, energy band model, density of states, distribution statistics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, - drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger, radiative, and surface.

UNIT II

Junctions p-n junctions: fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristic, steady state and transient conditions, capacitance model, reverse-bias breakdown, metal-semiconductor junctions fabrication, Schottky barriers, rectifying and ohmic contacts, I-V characteristics.

UNIT III

MOS Capacitors and MOSFETs : The MOS capacitor – fabrication, surface charge – accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao Sah and Schichman – Hodges models, I-V characteristic, second order effects – Velocity saturation, short-channel effects, charge 2 sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect.

UNIT IV

MESFETs : MESFETs fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics.

UNIT V

BJTs and HBTs: BJTs – fabrication, basic operation, minority carrier distributions and terminal currents, I-V characteristic, switching, second-order effects – base narrowing, avalanche multiplication, high-injection, emitter crowding, Kirk effect, etc.; breakdown, high-frequency response, Gummel-Poon model, HBTs: - fabrication, basic operation, technological aspects, I-V characteristics.

TEXT/REFERENCE BOOKS:

1. Ben G. Streetman, Solid State Electronic Devices, Prentice Hall, 1997.

2. Richard S. Muller and Theodore I. Kamins, Device Electronics for Integrated Circuits, John Wiley, 1986.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Advanced VLSI Design"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41112VL

Objectives: To understand different CMOS logic families and their circuit layout. To understand various VLSI design methodologies.

Course Content

UNIT I

Review of MOS transistor models. CMOS logic families including static, dynamic and dual rail logic, i.e., Parallel & Series Equivalent circuits; Static CMOS Circuit Design, High Speed Dynamic CMOS logic families; Precharge-Evaluate logic; Dynamic CMOS logic circuits, cascading, charge sharing and clock distribution.

UNIT II

Integrated Circuit Layout: Design Rules, Parasitic component in layout.

UNIT III

Memory/register, Structure Design; ROM Design, SRAM and DRAM Design, Building blocks: ALU's, FIFO's, counters.

UNIT IV

VLSI system design: data and control path design, floor planning,

UNIT V

Design methodology: Introduction to hardware description languages (VHDL), logic, circuit, and layout verification. Design examples.

TEXT/REFERENCE BOOKS:

1. Principles of CMOS VLSI Design, Addison Wesley N. Weste and K. Eshranghia Addison Wesley. 1985
2. The Design and Analysis of VLSI Circuits ,L. Glaser and D. Dobberpuhl ,Addison Wesley,1985
3. Introduction to VLSI Systems ,C. Mead and L. Conway ,Addison Wesley1979
4. Digital Integrated Circuits: A Design Perspective, J. Rabaey, Prentice Hall India, 1997
5. VHDL ,D. Perry, McGraw Hill International 1995 2nd Ed.,

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG

Department of Electronics and Telecommunication

"Introduction to CAD Tools"

Theory Periods: 30

Credits: 4

Tutorials: "

Code: ET41

Objectives: To familiar with spice for circuit simulation. To understand various techni for circuit design methodologies.

Course Content

UNIT I

Introduction, CAD and SPICE overview.

UNIT II

Understanding simulation, numerical integration, convergence, time step control. AC, DC and transient analysis.

UNIT III

Diode model, ideal diode, BJT model, MOSFET model, unified charge control model (UCCM), SPICE level 1, 2, and 3, and barkeley short-channel IGFET model (BSIM).

UNIT IV

HBT SPICE model, MESFET spice model, high frequency model.

UNIT V

Differential amplifier, current mirrors, active loads, Output stages, Op-Amps, compensation, Macro-modeling, and behavioral modeling.

TEXT/REFERENCE BOOKS:

1. "Semiconductor Device Modelling with SPICE", Giuseppe Massobrio and Paolo Antognetti, McGraw-Hill Inc.
2. "Inside SPICE, overcoming the obstacles of circuit simulation", Ron Kielkowski, McGraw-Hill Inc.
3. "SPICE for circuits and electronics using PSpice", Muhammad H. Rashid, Prentice Hall
4. Manual of suggested tools

Suggested tools/software:

1. Cadence design tools
2. Mentor Graphics
3. Xilinx ISE
4. Synopsis/Silvaco – TCAD
5. Tanner
6. IRSIM

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NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Digital IC Design"

Theory Periods: 30 Tutorials: "10"
Credits: 4 Code: ET41114VL

Objectives: To understand basics of hardware description languages. To implement various examples of digital IC designs using hardware description languages.

Course Content

UNIT I

Basic concepts of hardware description languages. Hierarchy, Concurrency, Logic, and Delay modeling, Structural, Data-flow and Behavioral styles of hardware description. Architecture of event driven simulators.

UNIT II

Variable and signal types, arrays, and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations. Component instantiation.

UNIT III

Use of Procedures and functions, Examples of design using Verilog and VHDL. Syntax and Semantics of Verilog. Variable types, arrays, and tables. Operators, expressions and signal assignments.

UNIT IV

Modules, nets and registers, Concurrent and sequential constructs. Tasks and functions, Examples of design using Verilog.

UNIT V

Synthesis of logic from hardware description.

TEXT/REFERENCE BOOKS:

1. VHDL,Z. Navabi,McGraw Hill International Ed. 1998
2. Verilog HDL: A Guide to Digital Design and Synthesis,S. Palnitkar,"Prentice Hall NJ, USA),1996
3. VHDL Primer,J.Bhaskar,Pearson Education Asia,2001
4. Verilog HDL Synthesis - A Practical Primer, "J.Bhaskar", Star Galaxy Publishing,(Allentown, PA)",1998
5 Verilog Digital System Design, Z. Navabi,McGraw Hill Education 2nd Ed. 2008

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 49

Department of Electronics and Telecommunication

"Design Lab - 1"

Theory Periods: 50

Code: ET41121VL

Credi

Objectives: To familiar with CAD and SPICE for device/circuit simulation. To understa various techniques for device/circuit design methodologies.

Course Content

- Use of CAD and SPICE for device/circuit design.
- Logic design and Layout design
- Circuit extraction from layout and verification by simulation of extracted circuits.

TEXT/REFERENCE BOOKS:

1. SPICE manual
2. IRSIM manual
3. MAGIC manual
4. Xilinx Corporation, "FPGA technology for Nineties" Xilinx Handbook, 1992.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Digital Design Lab"

Theory Periods: 50 Credits: 3
Code: ET41122VL
Objectives: To familiar with HDL simulation.
Course Content
• Experiments related to language semantics Time Control: delay operator, event control. Assignment Types: procedural, blocking, non-blocking, continuous. Delay through combinational logic and nets
• Behavioural Coding (examples and problems)
• Structural Coding (examples and problems)
• RT-Level Coding (examples and problems)
• Mixed-Level Coding (examples and problems)
• Coding of state machines and sequential logic
• Coding of test benches
• Coding style for synthesis
• Entering design constraints and synthesis using "FPGA Express" - Generating timing reports; CLB/gate usage reports; Identifying suitable FPGA device (Xilinix) for design implementation.
• A mini-project example and suggestions for mini-project topics.

TEXT/REFERENCE BOOKS:

1. G. De Micheli, Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.
2. P. Kurup and T. Abbasi, Logic Synthesis Using Synopsys, Second Edition, Kluwer, 1996.
3. J. Bhasker, A VHDL Primer, Third Edition, Prentice-Hall, 1999.
4. Z. Navabi, Verilog Digital System Design, McGraw-Hill, 1999.
5. S. Palnitkar, Verilog HDL : A Guide to Digital Design and Synthesis, Prentice-Hall, 1996.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 4

Department of Electronics and Telecommunication

"Analog IC Design"

Theory Periods: 30 Tutorials: "1

Credits: 4 Code: ET4121

Objectives: To study Basics of analog IC designing. To understand the Frequency respon stability and noise issues in amplifiers. To understand the implementation of linear and non linear analog block implementation and their testing.

Course Content

UNIT I

Basic Analog Building Blocks, Switches, Active Resistors, Current and Voltage sources, Current Mirrors, Current and voltage references, Voltage regulators

UNIT II

Amplifiers: Basic Amplifiers, Differential Amplifier, Cascode Amplifiers, High Gain Amplifier Structure, Amplifier design,

UNIT III

Operational Amplifiers: Operational Amplifier characteristics, Basic Op-Amp circuits, Frequency response and compensation,

UNIT IV

Noise sources in Op-Amps, Op-Amp design including Biasing circuits, High performance Op-Amps

UNIT V

Comparators: Single stage comparators, Two stage comparator, Comparators with Hysterisis, Auto zero techniques

TEXT/REFERENCE BOOKS:

1. "Analog MOS Integrated Circuits for Signal Processing", Roubic Gregorian and Gabor C. Temes, John Wiley & Sons, 1986.

2. "VLSI Design Techniques for Analog and Digital Circuits", Randall Geiger, Phillip E. Allen and Noel Stradder, McGraw Hill International Edition, McGraw Hill.

3. "CMOS Analog Circuit Design" Phillip E. Allen and Douglas R. Holberg.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Analog IC Design Lab"

Theory Periods: 30
Code: ET41221VL
Credits: 2

Objectives: To simulate basics of analog IC. To understand the Frequency response, stability, and noise issues in amplifiers. To understand the implementation of linear and nonlinear analog block implementation and their testing using simulation.

Course Content

Experiments based on Analog IC Design subject such as current and voltage sources, amplifiers, comparators etc.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"System-on-Programmable-Chip Design"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41212VL

Objective: Today, VLSI chips are entire "system-on-chip" designs, which include processors, memories, peripheral controllers, and connectivity sub-systems. The course aims to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow.

Course Content

UNIT I

Introduction: Driving Forces for SoC - Components of SoC - Design flow of SoC Hardware/Software nature of SoC - Design Trade-offs - SoC Applications

System-level Design: Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.

UNIT II

Interconnection: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-onchip: Architecture-topologies-switching strategies - routing algorithms flow control, Quality-of-Service- Re-configurability in communication architectures.

UNIT III

IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.

UNIT IV

SOC implementation: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.

UNIT V

SOC testing: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT).

TEXT/REFERENCE BOOKS:

1. Michael J.Flynn, Wayne Luk, "Computer system Design: Systemon-Chip", Wiley-India, 2012.

2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.

3. W.H.Wolf, "Computers as Components: Principles of Embedded Computing System Design", Elsevier, 2008.

4. Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, Springer, 2012.

5. Lin, Y-L.S. (ed.), "Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.

6. Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"System-on-Programmable-Chip Design Lab"

Theory Periods: 30 Credits: 2

Code: ET41222VL

Objective: Today, VLSI chips are entire "system-on-chip" designs, which include processors, memories, peripheral controllers, and connectivity sub-systems. The course aims to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow on system.

Course Content

(Can be designed around either Xilinx Microblaze / Altera NIOS /Open RISC + Wishbone) Implementation of basic SoPC using tools; interfacing with peripherals; creation of custom peripherals using HDL; enhancement of instruction set with custom instructions; optimizing system architecture through choice of processor enhancements – architecture exploration

To be structured around available sensor nodes or similar platform for cooperative functioning of multiple nodes; example: Wireless /Bluetooth Motes

FPGA platform: exploration of architectures; custom computing machines

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG

Department of Electronics and Telecommunication

"VLSI Systems Design"

Theory Periods: 30 Tutorials: [illegible]

Credits: 4 Code: ET41

Course Content

UNIT I

Essential features of Instruction set architectures of CISC, RISC and DSP processors a their implications for implementation as VLSI chips; CISC Instruction-set implementatio and RT-Level optimization through hardware flow-charting (without/with pipelining concepts); Microprogramming approaches for implementation of control part of the processor; Handling of Instruction boundary interrupts, Immediate interrupts and traps in processors; Pipelined implementation of RISC Instruction Sets; Benefits and problems of pipelined execution; Hazards of various types and pipeline stalling; Scheduling (static and dynamic) and forwarding to reduce/minimize pipeline stalls;

UNIT II

Implementation of DSP Instruction sets; Programmable and function specific architectures; Synthesis of DSP architectures; Scheduling and resource allocation for DSP architectures; Design of processing elements; Conventional, residue number, cordic and distributed arithmetic architectures; Issues in the design and implementation of Instruction sets for special applications (optimizing the H/W – S/W interface);

UNIT III

Different abstraction levels in VLSI design; Design flow as a succession of translations among different abstraction levels; Gajski's Y-Chart; Need for manual designing to move to higher levels of abstraction with automatic translation at lower levels of abstraction.

UNIT IV

Need to model and validate the design at higher-levels of abstraction and the necessity of HDLs that encompass several levels of design abstraction in their scope;

UNIT V

VHDL hardware description language: introduction and detail.

Verilog hardware description language: introduction and detail, Design flow for VHDL/Verilog based RTL/logic synthesis and behavioural synthesis approaches.

TEXT/REFERENCE BOOKS:

1. A.M. Dewey, Analysis and Design of Digital Systems with VHDL, PWS Kent, 1996.

2. A.A. Jerraya, H. Ding and P. Kission, Behavioral Synthesis and Component Reuse with VHDL, Kluwer, 1996.

3. K.C. Chang, Digital System Design with VHDL and Synthesis: An Integrated Approach, Wiley India Pvt. Ltd., New Delhi .

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NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Embedded Systems & RTOS"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41231VL

Objective: This course focuses on acquiring a deep knowledge of various 64-bit processors, its process architectures, instruction sets and interfacing with various peripherals.

Course Content

UNIT I

Software, Real-time models, periodic/aperiodic tasks, resource sharing.

UNIT II

RTOS, basic OS functions, task scheduling, prioritization, inter-task communications, interrupts, semaphores.

UNIT III

Event-driven systems, Processing and communication, system components, interconnects.

UNIT IV

Bus architectures, communication protocols, microcontroller and FPGA architectures and instruction sets, low-power design.

UNIT V

Hardware, models of hardware – FSM, controller, micro-programmed etc, architecture synthesis, design space exploration.

Lab:

• To be structured around available sensor nodes or similar platform for cooperative functioning of multiple nodes; example: Wireless / Bluetooth Motes

• FPGA platform: exploration of architectures; custom computing machines

TEXT/REFERENCE BOOKS:

1. Peter Marwedel: Embedded System Design
2. W. Wolf. Computers as components: principles of embedded computing system design. Morgan Kaufmann, 2012. 3. High-Performance VLSI Signal Processing: Innovative Architecture and Algorithms, Vol. 1 by K.J.Ray Liu and K.Yao, IEEE Press, 1998.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication Engineering

"Signal Processing Algorithms of DSP Architecture"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41232VL

Objectives: To provide sound foundation of digital signal processing (DSP) architectures and designing efficient VLSI architectures for DSP systems.

Course Content

UNIT I

Transformations for retiming: Folding and unfolding DSP programs. Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

UNIT II

Redundant arithmetic: redundant number representations, carry free radix 2 addition and subtraction, Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures, data format conversion. Redundant to nonredundant converter.Numerical strength reduction.

UNIT III

Synchronous pipelining: clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems.Asynchronous pipelining.

UNIT IV

Scaling versus power consumption: Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.

TEXT/REFERENCE BOOKS:

1. K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.
2. Proakis, Digital Signal Processing, PHI, Second edition.
3. Lars Wanhammar, DSP Integrated Circuits, Academic Press, First edition, 1999

K KParhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiely, 2007

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Mixed Signal IC Design"

Theory Periods: 30 | Tutorials: "10"

Credits: 4 | Code: ET41233VL

Objective: This course is to provide students with sound understanding of metal-oxide-semiconductor field-effect transistor and the relationship of process technology with models used for analog IC. CMOS digital circuits will be introduced and analyzed. It provides exposure to the complex, non-digital behavior of the devices and circuits with which digital systems are implemented. Emphasis is given on the circuit design, optimization, and layouts.

Course Content

UNIT I

Building blocks for CMOS amplifiers: design of current mirrors, differential amplifiers, CMOS operational transconductance amplifiers: design of single ended telescopic cascode, folded cascode and two-stage amplifiers.

UNIT II

Frequency compensation schemes: Miller compensation, Ahuja compensation and Nested-Miller compensation.

UNIT III

Design of fully differential amplifiers, discussion of common mode feedback circuits. Switched capacitor circuits, design of switched capacitor amplifiers and integrators, effect of opamp finite gain, bandwidth and offset, circuit techniques for reducing effects of opamp imperfections, switches and charge injection and clock feed-through effects.

UNIT IV

Design of sample and hold and comparators. Fundamentals of data converters; Nyquist rate A/D converters (Flash, interpolating, folding flash, SAR and pipelined architectures); Nyquist rate D/A converters - voltage, current and charge mode converters, hybrid and segmented converters); Oversampled A/D and D/A converters.

UNIT V

Design of PLL's and DLL's and frequency synthesizers.

TEXT/REFERENCE BOOKS:

1. R. Gregorian and Temes - Analog MOS integrated circuits for signal processing
2. R.Gregorian - Introduction to CMOS opamps and comparators.
3. D.Johns and K.Martin - Analog integrated circuit design
4. B.Razavi - Monolithic Phase-locked loops and clock recovery circuits: Theory and design.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Image Processing and Computer Vision"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41234VL

Objectives: To understand the role of digital image processing in the field of computer vision. To understand various mechanisms responsible for image segmentation, motion analysis, motion estimation, computational imaging and super resolution. To study and understand the 3-dimensional imaging mechanisms. To study and understand the image and video compression mechanisms. To understand the basics of color image processing. To study various applications of computer vision systems.

Course Content

UNIT I

Review of basics of Digital image processing, Introduction about computer vision: What is computer vision, advantages and disadvantages of computer vision, general applications of computer vision Feature detection and matching

UNIT II

Points and patches, edges, lines, Segmentations: Feature based alignment: 2D and 3D feature based alignments algorithms and applications, Pose estimation algorithms. Motion estimation: Differential motion analysis methods, optical flow, detection of specific motion patterns, image stitching, motion models for tracking, alignments, compositing.

UNIT III

Image and video Compression techniques. Computational imaging: super resolution, blur removal, image matting and compositing, texture analysis and synthesis, stereo imaging, basic concepts, and applications.

UNIT IV

3D image processing techniques: basics of 3D images, 3D sensing, camera calibrations, and reconstructions, 3D from 2D image, surface based representations, point based representations, and volumetric based representations, and model based reconstruction, recovering textures from 3D images and applications of 3D imaging techniques, 3D shape recognition.

UNIT V

Object Recognition techniques Basics Colour image processing: Color fundamentals, color models, color transformation, color segmentation, smoothing, and sharpening. Case studies of computer vision projects such as content-based image retrieval, face recognition etc.

TEXT/REFERENCE BOOKS:

1. "Computer Vision: Algorithms and Applications" by "Richard Szeliski"Springer, 2010
2. "Computer Vision", "Shapiro and Stockman," Prentice Hall, 2001
3. "Image Processing, Analysis, and Machine Vision", "Sonka, Hlavac, and Boyle" Cengage Learning, 2009.
4. "Fundamentals Of Machine Vision", by "Harley R. Myler" PHI Learning (2003)
5. "Computer Vision: A Modern Approach" by "Forsyth, David A., Ponce, Jean" PHI Learning (2009)
6. "Pattern Recognition and Image Analysis" by", " Earl Gose Steve Jost and Richard Johnsonbaugh", PHI (2009)
7. "Fundamentals of Digital image processing", by "Anil K. Jain", PHI, 2010
8. "Digital image processing", by Rafael C. Gonzalez and Richard E. Woods," Pearson Education 3rd Edition.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"VLSI Technology"

Theory Periods: 30 Tutorials: "10"
Credits: 4 Code: ET41235VL

Objectives: To study various VLSI fabrication steps such as oxidation, lithography, etc. To understand the process of VLSI circuit implementation.

Course Content

UNIT I

Solid state diffusion modeling and technology, ion implantation technology and damage annealing, characterization of impurity profiles.

UNIT II

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra-thin films, Oxidation oxidation techniques in VLSI and ULSI, characterization of oxides films, low k and high k dielectrics for ULSI.

UNIT III

Environment for VLSI Technology, Clean room and safety requirements, Wafer cleaning process and wet chemical etching techniques.

UNIT IV

Lithography: Photolithography, e-beam lithography and newer lithography techniques for VLSI/ULSI, mask generation. chemical vapor deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitrite and metal films, epitaxial growth of silicon. Metal film deposition: Evaporation and sputtering techniques, failure mechanisms in metal interconnect multilevel metallization schemes.

UNIT V

Plasma and rapid thermal processing, PECVD, plasma etching and RIE techniques, RTP techniques for annealing , growth and deposition of various films for use in ULSI

TEXT/REFERENCE BOOKS

1. VLSI Technology,S. M. Sze,McGraw Hill, II , 1988
2. VLSI fabrication principles, S. K. Gandhi,,"John Wiley, New York",1983
3. ULSI Technology,C. Y. Chang. S. M. Sze,McGraw Hill companies,1996

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Advanced Techniques in DSP"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41241VL

Course Content

UNIT I

PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION

Relationship between the auto correlation and the model parameters – The Yule – Walker method for the AR Model Parameters – The Burg Method for the AR Model parameters – unconstrained least-squares method for the AR Model parameters – sequential estimation methods for the AR Model parameters – selection of AR Model order.

UNIT II

ADAPTIVE SIGNAL PROCESSING

FIR adaptive filters – steepest descent adaptive filter – LMS algorithm – convergence of LMS algorithms – Application: noise cancellation – channel equalization – adaptive recursive filters – recursive least squares.

UNIT III

MULTIRATE SIGNAL PROCESSING

Decimation by a factor D – Interpolation by a factor I – Filter Design and implementation for sampling rate conversion: Direct form FIR filter structures – Polyphase filter structure.

UNIT IV

SPEECH SIGNAL PROCESSING

Digital models for speech signal : Mechanism of speech production – model for vocal tract, radiation and excitation – complete model – time domain processing of speech signal:- Pitch period estimation – using autocorrelation function – Linear predictive Coding: Basic Principles – autocorrelation method – Durbin recursive solution.

UNIT V

WAVELET TRANSFORMS

Fourier Transform : Its power and Limitations – Short Time Fourier Transform – The Gabor Transform - Discrete Time Fourier Transform and filter banks – Continuous Wavelet Transform – Wavelet Transform Ideal Case – Perfect Reconstruction Filter Banks and wavelets – Recursive multi-resolution decomposition – Haar Wavelet – Daubechies Wavelet.

TEXT/REFERENCE BOOKS:

1. John G.Proakis, Dimitris G.Manobakis, Digital Signal Processing, Principles, Algorithms and Applications, Third edition, (2000) PHI.
2. Monson H.Hayes – Statistical Digital Signal Processing and Modeling, Wiley, 2002.
3. L.R.Rabiner and R.W.Schaber, Digital Processing of Speech Signals, Pearson Education (1979).
4. Roberto Crist, Modern Digital Signal Processing, Thomson Brooks/Cole (2004)
5. Raghuveer. M. Rao, Ajit S.Bopardikar, Wavelet Transforms, Introduction to Theory and applications, Pearson Education, Asia, 2000.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"MOS Device Modeling and Characterization"

Theory Periods: 30 Tutorials: "10"
Credits: 4 Code: ET41242VL

Course Content

UNIT I

2-terminal MOS device: threshold voltage modeling (ideal case as well as considering the effects of Q_f, Φ_{ms} and D_{it}.).

UNIT II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Qm and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Qm and Dit)

UNIT III

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modeling (SPICE level 1,2,3 and 4).

UNIT IV

Subthreshold current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT V

SOI MOSFET: basic structure; threshold voltage modeling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics

TEXT/REFERENCE BOOKS:

1. D.G.Ong , "Modern MOS Technology: Processes, Devices and Design", McGraw Hill, 1984.
2. Y.Taur and T.H.Ning, "Fundamentals of modern VLSI Devices" Cambridge Univ. Press, 1998.
3. S.M.Sze, "Physics of Semiconductor Devices" Wiley,1981.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Security Solutions in VLSI"

Theory Periods: 30 | Tutorials: "10"
Credits: 4 | Code: ET41243VL

OBJECTIVES

1. To study the different kinds of threats to information security.
2. To know the various techniques for data encryption.
3. To introduce the fundamental concepts of authentication applications, Email security, IP Security and Web Security.
4. To formulate case study based on VLSI for security threats.
5. To design and implement the various cryptography algorithms in VLSI.

COURSE CONTENT

UNIT – 1: ENCRYPTION TECHNIQUES

Security Attacks, Services, and Mechanisms; Substitution Techniques: Caesar Cipher, Monoalphabetic Cipher, Playfair Cipher, Hill Cipher, Polyalphabetic Cipher, One-Time Pad; Transposition Techniques; Feistel Cipher Structure; Simplified DES (S-DES); Data Encryption Standard (DES); Double DES; Triple DES with two keys; Triple DES with three keys; Block Cipher Modes of Operation; Stream Ciphers and RC4; Finite Fields; AES (Advanced Encryption Standard); Introduction to Number Theory; The RSA Algorithm; Key Management; Diffie-Hellman Key Exchange; Message Authentication and Hash Algorithm: Authentication Requirements and Functions, Message Digest Algorithm (MD5), Secure Hash Algorithm (SHA-1, SHA-256); Digital Signatures and Authentication Protocols.

UNIT – 2: NETWORK SECURITY PRACTICE

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS, Authentication Applications – Kerberos – X.509 Authentication Service– Electronic Mail Security – Pretty Good Privacy – S/MIME– IP Security – IP Security Overview– IP Security Architecture – Authentication Header – Encapsulating Security Payload – Combining Security Associations – Web Security – Web Security Considerations – Secure Sockets Layer and Transport Layer Security – Secure Electronic Transaction .

UNIT – 3: FIREWALLS AND CYBER LAWS

Firewalls, Design Principles, Trusted Systems, IT Act and Cyber Laws, Virtual Private Network.

UNIT – 4: FUTURE THREATS TO NETWORK

Recent Attacks on Networks, VLSI based Case Study

UNIT – 5: CRYPTO CHIP DESIGN

VLSI Implementation of AES Algorithm, Implementation of DES, IDEA AES Algorithm, Development of Digital Signature Chip using RSA Algorithm.

REFERENCES:

1. William Stalling, "Cryptography and Network Security", Pearson Education, 2005.
2. Charels P. Pfleeger, "Security in Computing", Prentice Hall, 2006.
3. Jeff Crume, "Inside Internet Security", Addison Wesley, 2000.
4. Charlie Kaufman, "Network Security Private Communication in Public World" 2nd edition, Prentice Hall of India New Delhi, 2004.
5. William Stallings, "Network Security Essentials", 2nd edition, Prentice Hall of India ,New Delhi, 2004.
6. Bernad Menezes,Network Security and Cryptography",Cengage Learning Ist edition 2010.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Low Power Design Techniques"

Theory Periods: 30 Tutorials: "10"
Credits: 4 Code: ET41244VL

Objective: The objective of this course is to provide students with understanding of sources of power consumption of CMOS circuits. This course also discussed about Power Reduction Techniques and Low Power Logic design Styles.

Course Content

UNIT I

Introduction; Power Dissipation in CMOS MOSFETs.

UNIT II

Power Estimation.

UNIT III

Design of Low-Power CMOS Circuits.

UNIT IV

Low-Power SRAM/DRAM Design.

UNIT V

Software Design for Low Power.

TEXT/REFERENCE BOOKS:

1. J. B. Kuo and J-H. Lou, Low-Voltage CMOS VLSI Circuits, Wiley, 1999.
2. K. Roy and S. C. Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000
3. A. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design, Kluwer, 1995.
4. A. P. Chandrakasan and R. W. Broderson, Low-Power CMOS Design, IEEE Press, 1998.
5. E. Sanchez-Sinencio and A. G. Andreou, Low-Voltage/Low-Power Integrated Circuits and Systems : Low-Voltage Mixed Signal Circuits, IEEE Press, 1999.
6. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Second Edition, PH/Pearson, 2003.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"MEMS"

Theory Periods: 30 | Tutorials: "10"

Credits: 4 | Code: ET41245VL

Objectives: The Microelectromechanical devices are new generation devices which are used as the sensor, transducers and actuators. Many of these devices are being developed and they are replacing many bulky electro-mechanical devices. The fabrication technology design and analysis of these devices is the major part of this course.

Course Content

UNIT I

Historical Background: Silicon Pressure sensors, Micromachining, Micro Electro Mechanical Systems Micro-fabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining.

UNIT II

Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA) Physical Microsensors. Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors Microactuators :

UNIT III

Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector Surface Micromachining

UNIT IV

One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems : Success Stories, Micromotors, Gear trains, Mechanisms

UNIT V

Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

TEXT/REFERENCE BOOKS

1. Stephen D. Senturia, "Microsystem Design" by, Kluwer Academic Publishers, 2001.
2. Marc Madou, "Fundamentals of Microfabrication" by, CRC Press, 1997.Gregory Kovacs, "Micromachined Transducers Sourcebook" WCB McGraw-Hill, Boston, 1998.
3. M.-H. Bao, "Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes" by Elsevier, New York, 2000.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Power Device Modeling and application"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41331VL

Objectives: To study and familiarization of power devices. Power semiconductor devices are also important as low power devices.

Course Content

UNIT I

Review of conventional power devices IGBT, MESFET, HEMT.

UNIT II

Physics of power devices; power BJT, IGBT, MESFET, GaAs/GaN devices, power MOSFETs etc, and working principle of power devices.

UNIT III

Types of power MOSFETs, lateral, vertical, importing Superjunction concept in power devices, High-k, MOS devices and applications.

UNIT IV

Design of power MOSFETs using Wide-bandgap semiconductor materials such as GaAs, SIC, GaN etc.

UNIT V

Buck-boost convertors designing using power MOSFETs using SPICE.

TEXT/REFERENCE BOOKS

1. D. A. Grant and J. Grower, Power MOSFETs theory and application. John Wiley and Sons, 1989.

2. D. Neamen, Semiconductor Physics And Devices. McGraw-Hill Education (India) Pvt Limited, 2003.

3. S. K. Gandhi, VLSI Fabrication Principles Silicon and Gallium Arsenide, 2nd ED. Wile Student Edition, 2003.

4. B. J. Baliga," Advanced Power MOSFET Concepts". Springer, 2010.

5. B. J. Baliga, Silicon Carbide Power Devices. World Scientific Publishing Co. Pte. Ltd., 2005.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"RF IC Design"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41332VL

Objectives: To understand issues involved in design for GHz frequencies. To understand theoretical background relevant for design of active and passive circuits for RF front end in wireless digital communication systems.

Course Content

UNIT I

Characteristics of passive components for RF circuits. Passive RLC networks. Transmission lines. Two-port network modeling. S-parameter model. The Smith Chart and its applications.

UNIT II

Active devices for RF circuits: SiGe MOSFET, GaAs pHEMT, HBT and MESFET. PIN diode. Device parameters and their impact on circuit performance. RF Amplifier design: single and multi-stage amplifiers.

UNIT III

Review of analog filter design. Low-pass, high-pass, band-pass and band-reject filters. Bandwidth estimation methods. Voltage references and biasing. Low Noise Amplifier design: noise types and their characterization, LNA topologies, power match vs noise match.

UNIT IV

Linearity and large-signal performance. RF Power amplifiers: General properties. Class A, AB and C Power amplifiers. Class D, E and F amplifiers. Modulation of power amplifiers.

UNIT V

Analog communication circuits: Mixers, phase-locked loops, oscillators and synthesizers. Design and performance characterization. Tran-receiver design

TEXT/REFERENCE BOOKS

1. The Design of CMOS Radio Frequency Integrated Circuits, Lee Thomas H, Cambridge University Press.
2. Design of Analog CMOS integrated circuits, Razavi Behzad, McGraw Hill
3. VLSI for wireless communication, Bosco Leung, Pearson Education

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010
Department of Electronics and Telecommunication
"Design for Test Ability, Yield and Reliability"

Theory Periods: 30 Tutorials: "10"
Credits: 4 Code: ET41334VL

Objective: To understand basic concepts of testing and verification of VLSI design process. To understand the fundamentals of VLSI testing. To understand various approaches for system testing.

Course Content

UNIT I

Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs.

UNIT II

Fundamentals of VLSI testing. Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan.

UNIT III

System testing and test for SOCs. Iddq testing. Delay fault testing. BIST for testing of logic and memories.

UNIT IV

Test automation. Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification.

UNIT V

Basics of equivalence checking and model checking. Hardware emulation. Parametric testing, Reliability modeling, Yield models.

TEXT/REFERENCE BOOKS:

1. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers,2000
2. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design, IEEE", IEEE Press, 1990
3. T. Krop, "Introduction to Formal Hardware Verification", Springer Verlag,,2000
4. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
5. Jan M. Rabaey, "Digital Integrated Circuits", Prentice Hall, 2003.
6. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson Education India, 1997
7. Alfred L. Crouch "Design for test for digital ICs and embedded core systems" , PHI 1999.

NATIONAL INSTITUTE OF TECHNOLOGY, RAIPUR, CG 492010

Department of Electronics and Telecommunication

"Nano Electronics"

Theory Periods: 30 Tutorials: "10"

Credits: 4 Code: ET41333VL

Objectives: Nanoelectronics the aggressive scaling of CMOS devices resulted in the reduction of dimensions of active devices in the nanometer region. At the same time research has also being done to fabricate devices with different methodology and also the with different materials and not limited to silicon. In this course modeling aspects of these devices are discussed from perspective of circuit applications.

Course Content

UNIT I

Shrink-down approaches: Introduction, CMOS Scaling,

UNIT II

The nanoscale MOSFET, FinFETs, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunneling Transistors.

UNIT III

Single electron transistors, new storage, optoelectronic, and spintronics devices.

UNIT IV

Atoms-up approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics, molecular interconnects.

UNIT V

Carbon nanotube electronics, band structure & transport, devices, applications

TEXT/REFERENCE BOOKS:

1. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens,Wileyÿ (2003), C.P. Poole Jr.,F.J. Owens,Wiley (2003).
2. Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Waser Ranier ,Wiley-VCH,2003
3. Nanosystems, K.E. Drexler,Wiley (1992),1992
4. The Physics of Low-Dimensional Semiconductors,John H. Davies,"Cambridge University Press, "1998