TEQIP Sponsored
Short Term Training Program (STTP)
on
"Workshop on VLSID-SoC & Micro-nano Technologies"

26 to 30 September, 2016

REGISTRATION FORM

Name: ……
Designation: ……..……
Organization: ……
Qualification: ……
Correspondence Address: ……
…….....
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Tel. (O) …… (R) …..……....
(M) ……..……....
E-Mail: ……..…….
DD Details:
Amount …….....
No.....Date ……
Name of the Bank
…….
Accommodation Required: Yes / No

Date: Place:

Signature

Note:

1. Demand draft should be made in favour of **Director, NIT Raipur**, payable at Raipur.
2. Original/Scan copy of "DD along with the registration-from must reach to the coordinators on or before **20th September, 2016"**.
3. A PDF copy of registration form can be downloaded from the institute website www.nitrr.ac.in

CHIEF-PATRON
Prof S Tiwari
Director, NIT Raipur

PATRON
Prof S Sanyal
Dean (R&C), NIT Raipur

COORDINATORS
Prof S Verma
Professor

Dr B Acharya Assistant Professor
Dr A Naugarhiya Assistant Professor

ORGANIZING COMMITTEE

Prof S Verma, Dr B Acharya, Mr S Chakroborty, Dr S K Saha, Mr R K Chaurasiya, Dr A S Raghuvanshi, Mr S Majumder, Mr A Gupta, Dr T Meenpal, Dr A Naugarhiya

INVITED SPEAKERS (Tentative)

Prof R M Patrikar, VNIT Nagpur
Prof P N Kondekar, IIITDM Jabalpur
Prof R B Deshmukh, VNIT Nagpur
Dr R Vaddi, IIIT-NR Raipur
Dr C K Sahu. MNIT Jaipur

ADDRESS FOR CORRESPONDENCE

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Department of Electronics and Telecommunication

National Institute of Technology, Raipur
G.E. Road, Raipur, India-492 010
Website: www.nitrr.ac.in

TEQIP-II Sponsored One Week Short Term Training Program on

Workshop on VLSID-SoC & Micro-nano Technologies

26th to 30th September, 2016

Organized by

Department of Electronics and Telecommunication Engineering

National Institute of Technology Raipur, India-492 010

ABOUT THE INSTITUTE

National Institute of Technology Raipur situated in the capital of Chhattisgarh, has proven to be "avant-grade" in the field of science and technology over past few decades in this region. With sweet memory of foundation ceremony by our president Hon'ble Dr. Rajendra Prasad on 14th September 1956, the institute started with two departments namely Metallurgical and Mining Engineering. Later the inauguration of the Institute building was done by our Prime Minister Hon'ble Pt. Jawahar Lal Nehru on 14th March 1963. From 1st December 2005, the institute has become the National Institute of Technology. It is well connected with Mumbai, Delhi and all metro cities by regular flights and is on the main Howrah-Mumbai railway route. The institute is 5 km from the Raipur railway station and 18 km from airport on NH-6, the Great Eastern Road.

ABOUT THE DEPARTMENT

The **Department of Electronics and Telecommunication** came into existence in 1985. The department aims be a national leader in imparting quality education, carrying out research and technology development in the field of Electronics and Telecommunication Engineering. The department provides an outstanding research environment and offers academic program leading to the award of B.Tech, and Ph.D. degree.

VENUE

Department of Electronics and
Telecommunication Engineering
NIT Raipur (CG) – 492 010, INDIA

OBJECTIVES

VLSID-SoC & Micro-nano Technologies which include Microelectronics & VLSI Design, System on Chip design & development and nano electronics have a significant role in engineering and manufacturing field across all engineering disciplines.

As such, it has wide applications in various program recently launched by Govt. of India, for example; Make in India, Smart Cities, Digital India etc.

The aim of this training programme is to provide an exposure to both basics and recent advances in VLSI and Micro-nano Technologies to the teaching and research community associated with the Departments of Electronics, Electrical and Computer Science etc.

Expert lectures will be delivered by faculty and scientists from various academic institutes, including IISc, IITs, IIITs, NITs and the host institute (NIT Raipur). Hands-On Sessions will be suitably designed to supplement classroom discussions using EDA tools.

ELIGIBILITY

Participation in this short term training programme (STTP) is open to the under-graduate students, post- graduate students, faculty members, engineers, researchers, and other executives working on diverse fields in Electronics Engineering, Computer Engineering, Electrical Engineering, Instrumentation Engineering, Biomedical Engineering, Biotechnology, etc.

SELECTION

The course coordinators reserve the right of selection of participants. The preference will be given to the participants from outside the institute (NIT Raipur). Intimation regarding selection will be sent to the candidates via email as per the schedule. Certificates will be issued to the participants only after attending the complete course. No TA/DA will be paid to the participants. However, paid accommodation may be provided to outside candidates at the institute hostels, provided request for the same is made in the registration form, well in advance.

TOPICS TO BE COVERED

- Introduction of VLSI & Micro-Nano Technology.
- IoT and Application in Smart City.
- ASIC Design Flow
- Circuit and System Design challenges for IoT Applications
- Emerging technologies and Circuit techniques for Ultra-low power Logic and Memory design
- Digital, Analog and RF circuit design using Nano scale Devices
- Low Power Advanced Semiconductor Device like JLFET, Silicon nanowire FET, Tunnel FET etc
- Semiconductor Fabrication Facilities and its scope in India
- High Band-gap Devices
- Charge Plasma based Devices

IMPORTANT DATES

Registration
On or before **20.09.2016,**

Intimation of acceptance
On or before **22.09.2016**,

REGISTRATION FEE DETAILS

Participants	Amount (in Rs)
UG Students	**500/-**
PG/PhD Students	**1000/-**
Faculty	**2000/-**
Industry Delegates	**3000/-**

Application in the prescribed format with registration fee in the form of Demand Draft drawn in favor of "**Director, NIT Raipur**" must reach the coordinator on or before **20 September, 2016.** Registration fee includes registration kit, tea and lunch during the program. **Fee is non-refundable for selected candidates.**